Model paper

ADIKAVI NANNAYA UNIVERSITY, RAJAMAHENDRAVARAM

CBCS/Semester System (w.e.f. 2015-16 admitted batch)

B.Sc., (THREE YEAR EXAMINATIONS)

SEMESTER-III – **ELECTRONICS**

Paper-III: Digital Electronics

Time: 3 Hrs Max. Marks: 75

PART – A

Answer any **FIVE** questions. 5 X 5 = 25 Marks

1. Convert the following decimal numbers into binary.
   (1). 1025 (2). 347
2. How NAND gate can be used as universal gate?.
3. State and prove De Morgan's laws.
4. Draw the circuit diagram of Half adder circuit and explain it.
5. Explain the operation of Multiplexer circuit.
6. Explain the working of T flip-flop.
7. Explain the working of shift right register.
8. Depict a note on ROM.

PART – B

Answer **ALL** questions. 5 X 10 = 50 Marks

9. With suitable examples, explain how subtraction can be done using 1's and 2's complements.

   or

   Explain the procedure with example the conversion of gray code to excess-3 code.
10. Explain sum of products (SOP) and product of sums (POS) methods of logic circuit designing.

    or

    What is Karnaugh map?. Illustrate the formation of four variable Karnaugh map.
11. With circuit diagram, explain the working CMOS NOR gate.

    or

    Explain the operation of three-input TTL NAND gate.
12. Explain the working of Master Slave flip-flop with truth table.

    or

    With circuit diagram explain the operation of mod-10 counter.
13. Explain the working of Programmable Logic Array.

    or

    Explain the working of Programmable Array Logic.